## **Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of the claims in the application:

## **Listing of Claims:**

- (Currently Amended) A <u>computer-implemented</u> method, comprising:
   maintaining a global resource namespace including a list of a plurality <u>of</u> child
   and parent resource objects <u>of an integrated circuit</u> and a representation of the
   relationships among the child and parent resource objects; and
   rebalancing the plurality of resource objects.
- 2. (Original) The method of claim 1, wherein rebalancing the plurality of resource objects includes recalculating available resources.
- 3. (Original) The method of claim 2, wherein rebalancing the plurality of resource objects includes determining whether the available resources are less than currently consumed resources.
- 4. (Original) The method of claim 3, wherein rebalancing the plurality of resource objects includes allocating a temporary namespace if the available resources are less than the currently consumed resources.

- 5. (Original) The method of claim 4, wherein rebalancing the plurality of resource objects includes for each child resource object determining whether the child resource object has an owner.
- 6. (Original) The method of claim 5, wherein rebalancing the plurality of resource objects includes performing an attachment routine for each child object that is found to have an owner.
- 7. (Original) The method of claim 6, wherein rebalancing the plurality of resource objects includes destroying the old global resource namespace.
- 8. (Original) The method of claim 7, wherein rebalancing the plurality of resource objects includes renaming the temporary namespace to become a new global resource namespace.
- 9. (Original) A machine-readable medium having stored thereon instructions which, when executed by a computer system, causes the computer system to perform a method comprising:

maintaining a global resource namespace including a list of a plurality child and parent resource objects and a representation of the relationships among the child and parent resource objects; and

rebalancing the plurality of resource objects.

- 10. (Original) The machine readable medium of claim 9, wherein rebalancing the plurality of resource objects includes recalculating available resources.
- 11. (Original) The machine readable medium of claim 10, wherein rebalancing the plurality of resource objects includes determining whether the available resources are less than currently consumed resources.
- 12. (Original) The machine readable medium of claim 11, wherein rebalancing the plurality of resource objects includes allocating a temporary namespace if the available resources are less than the currently consumed resources.
- 13. (Original) The machine readable medium of claim 12, wherein rebalancing the plurality of resource objects includes for each child resource object determining whether the child resource object has an owner.
- 14. (Original) The machine readable medium of claim 13, wherein rebalancing the plurality of resource objects includes performing an attachment routine for each child object that is found to have an owner.
- 15. (Original) The machine readable medium of claim 14, wherein rebalancing the plurality of resource objects includes destroying the global resource namespace.

- 16. (Original) The machine readable medium of claim 15, wherein rebalancing the plurality of resource objects includes renaming the temporary namespace to become a new global resource namespace.
  - 17. (New) An apparatus comprising:

    an integrated circuit including a plurality of shared resources; and
    means for managing the plurality of shared resources.
- 18. (New) The apparatus of claim 17, further comprising means for managing a bandwidth of the plurality of shared resources in real-time.
- 19. (New) The apparatus of claim 17, wherein the integrated circuit comprises a graphics memory controller chipset.
- 20. (New) The apparatus of claim 19, further comprising a shared memory coupled to the graphics memory controller chipset.